Abstract of the Disclosure:

In a semiconductor device of a polysilicon gate electrode structure having three or more different Fermi levels, a P type polysilicon having a lowest Fermi level is disposed on a first N type surface channel MOS transistor. A first N type polysilicon having a highest Fermi level is disposed on a second N type surface channel MOS transistor. A second N type polysilicon having an intermediate Fermi level between the highest and the lowest Fermi levels and doped with both an N type impurity and a P type impurity is disposed on a P channel MOS transistor.